What is claimed is:

1. A method for forming an interconnect structure on a semiconductor body, comprising the steps of:

(a) depositing a first metal layer on a semiconductor body;

(b) depositing a sacrificial layer on the first metal layer, said sacrificial layer having a height;

(c) patterning the sacrificial layer and the metal layer to form separate metal lines with a sacrificial layer cap on said metal lines;

(d) depositing a low-k material to fill gaps between metal lines and to cover the sacrificial layer;

(e) removing the low-k material to a level within the height of the sacrificial layer;

(f) removing the sacrificial layer; and

(g) depositing a protective layer to cover the metal lines and the low-k material.

2. The method of claim 1, wherein the step of removing the low-k material to a level within the height of the sacrificial layer includes the step of etching back the low-k material to a level within the height of the sacrificial layer.

3. The method of claim 2 wherein step of etching back the low-k material to a level within the height of the sacrificial layer includes a plasma etch step.

4. The method of claim 1, wherein the step of removing the low-k material to a level within the height of the sacrificial layer includes the step of polishing the low-k material to a level within the height of the sacrificial layer.

5. The method of claim 4, wherein the step of polishing the low-k material to a level within the height of the sacrificial layer includes a chemical mechanical polish (CMP) step.

6. The method of claim 1, wherein the step of removing the low-k material to a level within the height of the sacrificial layer includes the steps of polishing the low-k material and etching back the low-k material.

7. The method of claim 6, wherein the steps of polishing the low-k material and etching back the low-k material includes a plasma etch step and a chemical mechanical polish (CMP) step.

8. The method of claim 1, further comprising the steps of:

depositing an insulator on the protective layer;

creating vias in the insulator;

performing a photoresist strip; and

performing a set clean.

9. The method of claim 8, further comprising selectively etching the protective layer.

10. The method of claim 9, wherein selectively etching the protective layer further includes the step of utilizing an isotropic etch.

11. The method of claim 9, wherein selectively etching the protective layer further includes the step of utilizing an an-isotropic etch to leave a spacer on a vertical portion of the low-k material in the vias.

12. The method of claim 9, further comprising filling the vias with a metal.

13. The method of claim 12, further comprising depositing and patterning a second metal layer over the insulator.

14. The method of claim 13, wherein the sacrificial layer is made of a material selected from the group consisting of an oxide, silicon oxide, aluminum oxide, silicon nitride, silicon carbide, a polymer, an organic material, a conductive material, titanium, titanium nitride, tungsten, tungsten nitride, and poly-silicon.

15. The method of claim 9, further comprising simultaneously depositing the plug metal and second metal layer at the same time, followed by patterning of the second metal layer.

16. An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling the gaps between the metal lines and having a height and one or more vertical portions;

(c) a protective layer formed over the metal lines and the low-k material, wherein the protective layer covers at least one vertical portion of the low-k material;

(d) a dielectric layer formed over the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal in the vias to contact the first metal lines.

17. The interconnect of claim 16, wherein the protective layer includes an oxide.

18. The interconnect of claim 17, wherein the oxide includes silicon dioxide.

19. The interconnect of claim 16, wherein the protective layer includes a dielectric material.

20. The interconnect of claim 19, wherein the protective layer includes silicon nitride.

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21. The interconnect of claim 16, wherein the protective layer includes silicon carbon. Carbide

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22. The interconnect of claim 16, further comprising a spacer disposed on the vertical portion of the low-k material in the vias. Antecedent okay

23. The interconnect of claim 16, wherein the protective layer is silicon nitride.

24. The interconnect of claim 16, wherein the first metal layer is an aluminum alloy, the metal filling the vias is tungsten, and the second metal layer is an aluminum alloy. tungst

25. The interconnect of claim 16, wherein the first metal layer is an aluminum alloy, the metal filling the vias is an aluminum alloy, and the second metal layer is an aluminum alloy.

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26. The interconnect of claim 16, wherein the dielectric layer is made of silicon dioxide, the protective layer is silicon nitride, and the low-k material is an organic low-k material.

27 The interconnect of claim 16, wherein the dielectric layer is made of silicon dioxide, the protective layer is silicon nitride, and the low-k material is a porous silicon dioxide.

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add B1

add H2

add D3